GAAS INTEGRATED CIRCUIT MANUFACTURING TECHNOLOGY COMES OF AGE

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ABSTRACT - Until very recently the efficacy of GaAs integrated circuit manufacturing technology could not be judged or measured against traditional Si integrated circuit standards. GaAs wafer processing volumes were limited (10-20 wafers/week), yields were unpredictable, reliability standards did not exist and industry standard manufacturing methodologies were not applicable. Since GaAs materials, processes and 1 μm design rules were unlike Si, early development efforts did not capitalize on Si integrated circuit approaches. Today, the establishment of high yield "Si-like" GaAs integrated circuit manufacturing technology closely paralleling silicon fabrication, testing and packaging approaches have become a reality. Practical commercial production has been realized through the use of high quality three inch GaAs wafers, cassette to cassette process equipment, direct step on wafer photolithography systems, dry processing techniques, parametric test equipment, automatic packaging equipment and custom GaAs high speed testing systems. The manufacturability and maturity of 1 μm depletion-mode GaAs ICs is routinely evident in day to day volume (140 wafers/week)production of MSI (~ 200 gates) circuits. Application of modern production methods after ~ two years of commercial experience are providing reproducible GaAs device parameters with outstanding characteristics and excellent wafer sort and high speed package yields.

Technology Introduction

GaAs materials for integrated circuit applications have been under intensive technology development for the past ten years. Interest in this technology has been due primarily to performance advantages realized from basic material properties of GaAs; mainly high electron mobility, high saturation velocity, wide band gap and semi-insulating substrate.[1] These superior electronic properties allow circuits fabricated on GaAs to operate typically five to ten times faster than silicon integrated circuits and at power levels two to five times lower. In addition, GaAs ICs are more radiation tolerant and can operate at higher temperatures than silicon, making them very attractive for military and other special environmental applications.

Commercial GaAs integrated circuits were first introduced in 1984 by GigaBit Logic and Harris Microwave. The viability of these early commercial efforts can be measured against the progress which has been made in pioneering manufacturing techniques, establishing reliability standards and obtaining customer and market credibility for GaAs ICs through introduction of ~ 20 MSI logic circuits.

The potential difficulties in establishing a manufacturing base for GaAs can be better understood by comparing the differences between GaAs and Si technology.[2,3,4] Table 1 contains a summary of the key differences between Si and GaAs technologies. Since GaAs has a wide energy band gap (1.4eV), bulk "semi-insulating" substrates with > 10^6 Ω-cm resistivities are possible. Therefore device isolation is directly provided by the substrate and parasitic capacitance is lower. While the semi-insulating feature of the GaAs substrate is advantageous, careful qualification of the substrate material is mandatory in order to obtain reproducible implantation and maintain device isolation during high temperature processing steps. The higher election mobility and saturation velocity of GaAs is key to the higher speed performance of GaAs over Si. Therefore the advantage of the high mobility must be preserved through various process steps. Of particular importance is complete removal of the implant damage requiring temperatures in excess of 800°C. This is a critical step in GaAs processing since GaAs dissociates above 600°C. Thus the GaAs surface must be encapsulated with a high quality dielectric such as silicon nitride.

Table 1 - Comparison of GaAs and Silicon Technology

	GaAs	Silicon
Material:		
Resistivity	Semi-Insulating>10^6Ωcm	Semi-Conductive
Energy Gap	1.4 eV	1.1 eV
Mobility(μ_e)	5000 cm^2/V-s	1000 cm^2/V-s
Technology:	No MOS or Diffusion Fully Ion Implanted Schottky Barriers	MOS/Bipolar Implanted/Diffused No Schottky Barriers
Lithography:	DSW/All Dry Etch 1 μm Design Rules 0.25 μm Overlay	Wet/Dry Etch ≥ 1.25 μm Rules ≥ 0.5 μm Overlay
Metals:	All Gold Based Ti, Pt, Au, AuGe, Ni	Al, Poly-Silicon Silicides

GaAs IC fabrication has been strictly limited to implantation and deposited dielectrics since neither n^- type diffusions or stable native oxides are available. Therefore MOS devices are not currently utilized (due to high surface states) in GaAs and Bipolar devices are a long way from maturity since a GaAs Bipolar device requires the use of complicated heterojunction structures.[5] Currently all GaAs ICs utilize implanted Schottky-barrier FETs and diodes. Unlike Silicon, high quality

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Schottky barriers in GaAs are readily obtainable.

The high speed performance requirements for GaAs necessitates the use of ultra small geometry devices. Standard design rules for GaAs are < 1μm gate lengths typically used in conjunction with 0.25 μm registration. These device geometry constraints dictate the use of an all wafer stepper and all dry processing technology. Such a strict adherence to state-of-the-art IC fabrication techniques throughout is not yet common to silicon production lines.

Contact and interconnect metals in GaAs technology are all Gold based. Gold based metalizations are used since the preferred ohmic contact to GaAs is an alloyed AuGe and the most reliable Schottky barrier is Ti/Pt/Au. These materials along with the fine line geometries require different deposition and replication techniques than those found in Si processing environments.

On the negative side, technical differences between Si and GaAs have prevented GaAs IC efforts from capitalizing on the specific learning curve and materials and circuit knowledge base established in Si ICs. Therefore, in a number of areas GaAs IC technology has had to come up the learning curve to a large degree on its own merit.

On the positive side, the trend towards a commonality in planar "Si-like" fabrication approaches and convergence of Si and GaAs processing equipment requirements necessary to produce ultra dense, micron resolved geometries has contributed to the excellent progress made in GaAs manufacturability.

GaAs IC Process

High performance GaAs ICs require MESFETS with shallow (< 2000 Å) layers, short (< 2 μm) channels, short (< 1 μm) gates, and narrow (~ 4 μm) metal pitches. This requires state-of-the-art processing at all levels including multiple selective ion implants, 10X reduction step and repeat projection lithography, and dry (plasma and ion beam) etching. Furthermore, to protect the integrity of GaAs Schottky barrier and Ohmic metal contacts requires low temperature (< 300°C) PE-CVD deposition techniques for the interlevel dielectric and final passivation.

Initally the GaAs wafers are cleaned and etched to provide an oxide free surface for the first critical dielectric deposition (see Figure 1). A thin sputtered Si_3N_4 cap is immediately deposited. This cap serves three purposes: 1) it prevents the decomposition of the GaAs at the anneal step (850°C), 2) prevents the formation of free surface states in the channel between gate and drain or source, and 3) prevents performance degradation during use over long periods of time. Si atoms are then implanted (n^- implant) through this cap to a depth of ~ 1700 Å at a dose of ~ 3 X 10^{12} atoms/cm^2 followed by a second Si implant (n^+ implant) to a depth of ~ 4000 Å at a dose of 5 X 10^{12} atoms/cm^2 for the source and drain regions. The n^+ implant reduces the channel length to ~ 1.8 μm providing low source resistance and improved Ohmic contact resistance. Wafers are then annealed (850°C) in order to remove the post implant damage. Ohmic contact windows are plasma etched to the GaAs surface and dieletric assisted liftoff[6,7] techniques are used to define the Au-Ge Ohmic contacts. The contacts are alloyed at temperatures of ~ 450°C. The Schottky (Ti/Pt/Au) contacts and first level interconnects are formed concurrently also using plasma etching and dielectric assisted liftoff. The metal thickness is chosen such that the openings in the dielectrics and metal are of ~ equal height resulting in a planar surface. The first metal pitch is 3.5 μm . A PE-CVD SiO_2 inter-layer is deposited through which the via windows are etched. The vias are then filled with Ti/Au using the enhanced liftoff process eliminating the need for sloped vias and maintaining minimum via dimensions of 2 μm X 2 μm . DC Magnetron sputtered Ti/Au is used for the second level of metallization which is patterned to a 4 μm pitch using ion-milling techniques. A final passivation layer of PE-CVD Si_3N_4 is deposited and plasma etched to open the saw-street and bond pads completing the process.

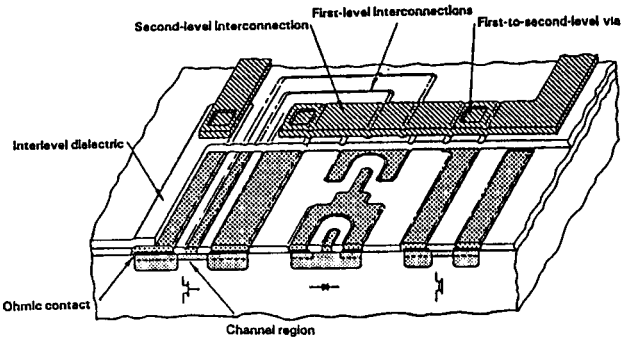

Fig. 1. Cutaway view of a planar GaAs IC.

With such small features and pitches, very high resolution (0.8 μm) and tight alignment overlay (mean + 3 σ < 0.25 μm) are required. This can be achieved today only through the use of 10X reduction steppers with auto-align capability. In addition, MESFET threshold limits requires the cap composition and thickness to be duplicated to an extrodinary degree (±30 Å). The extremely tight control required of this process necessitates the use of extensive process control monitoring.

Process Control

Over the past twenty months several thousand GaAs wafers have been fabricated, providing for the first time, significant statistical results for assessing GaAs IC manufacturability. The fabrication line at GigaBit is believed to be the first 3 inch GaAs cassette to cassette line in sustained operation of over 100 wafers/week. Work in process (WIP) is typically ~ 400 wafers with the average cycle time of 20 days. This level of production volume has been a significant step forward for GaAs IC technology.

As in Si IC manufacturing, GaAs fabrication at GigaBit benefits from careful tracking and analysis of process control monitors (PCM's). PCM tests cover the full spectrum of both individual process steps as well as all of the key device parameters. In the process control area measurements are made and recorded for all thin film deposition steps, implantation steps, photolithography,

etching, and lift-off steps. Strict adherence to statistical tracking methods like $\bar{X}/R$ charts has resulted in a well controlled stable process.

One key area that is critical to GaAs IC's based on 1 µm gate FETs is the precise control of photolithography resolution and subsequent feature replication. GaAs circuit performance is closely tied to short gate lengths (≤1um) and precise gate alignment between the implanted source and drain regions. Final Schottky barrier (Ti/Pt/Au) gate critical dimensions (CD's) are a result of controlling both the 1-µm photolithography resolution and the subsequent plasma etching and evaporated metal lift-off processes. Final gate lengths are routinely monitored; a histogram of nominally 1 µm metal gate lengths for 105 wafers is shown in Figure 2. These measurements are made on 3 fields on randomly selected wafers. This data supports the excellent control attainable using a Perkin-Elmer/Censor wafer stepper in conjunction with dry plasma etching. The mean of the gate length is 0.91 µm with a one sigma variation of 0.12 µm . Furthermore, the gates must be precisely centered in the ~ 1.8 µm long (n^-) channel to avoid threshold shifting from the adjacent (n^+) regions. This is achieved through auto-alignment features which maintain overlays of (mean + 3 σ) ±0.25 µm .

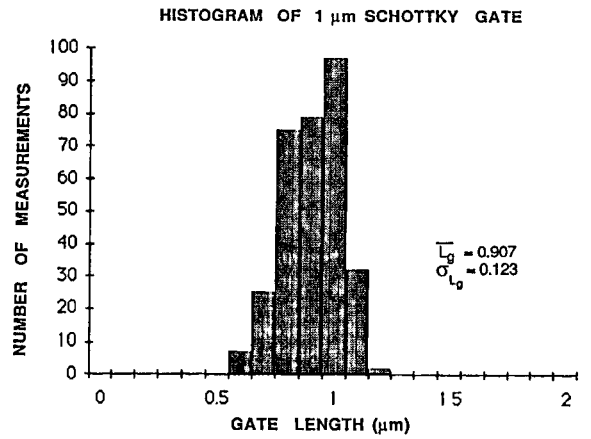

Fig. 2. Histogram of 1µm Schottky gate.

In addition to specific "in process" monitors, device parametric data is taken on 32 sites on each wafer after final device passivation. Measurements are made on FETs, active loads, diodes, ohmic contacts, sheet resistances, isolation, and backgating. This systematic parametric data collection of material and device statistics has provided the data to assess manufacturability.

Of paramount importance for active layer control and reproducibility is the quality of semi-insulating GaAs material. Both adequate GaAs material quality and supply has been attainable from several GaAs vendors both domestic and foreign. Pinch-off voltage (thresholds) variations are typically maintained at less than 150 mV across full GaAs ingots. Threshold voltage control over 517 wafers from 60 IC lots and ~ 10 different ingots is shown in Figure 3. The threshold target for these IC wafers is 1.0 volt. As can be seen from the pinch off voltage trend chart, a mean threshold of 0.958 V with a 1 sigma of ±0.155 mV was obtained. This level of control is very adequate for GaAs depletion-mode technology.

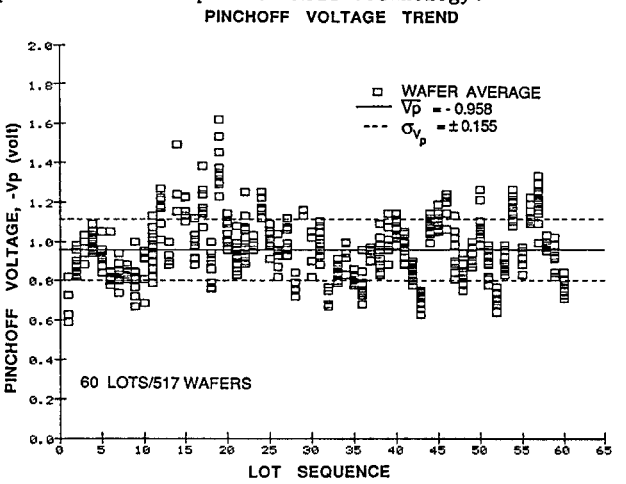

Fig. 3. Pinchoff voltage trend for 50 µm wide MESFET.

In addition to threshold reproducibility from wafer to wafer, uniformity across wafers is also important. Average threshold standard deviations for 1.0 volt devices, over full three inch wafers is typically 55-60 mV. The best lots average ~ 40 mV and the best wafers 22 mV. Figure 4 shows a threshold voltage histogram of a wafer exhibiting a $\bar{V}_p$ = -1.05 volt and 1 σ of ±38 mV. This result is not consistant with reports of high threshold variations due to the high dislocation densities typical on LEC GaAs wafers. The threshold voltage uniformity (< ±5%) obtainable for a -1.0 volt D-MESFET, when scaled to (+0.15 V) E-MESFET threshold requirements may be adequate to support enhancement technology. It would appear that the more formidable problem is reproducing the threshold voltages on each wafer. This observation suggests that GaAs technology development efforts should focus more strongly on FET threshold adjustable processes.

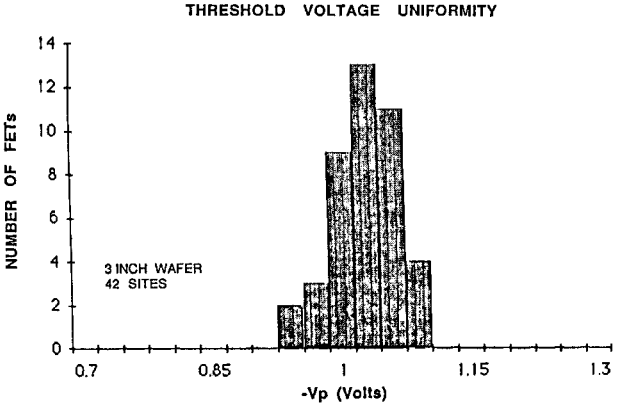

Fig. 4. Pinchoff voltage uniformity of 50 µm wide MESFETs on a 3" GaAs wafer.

Circuit Performance And Yield

Using the technology described in this paper, fourteen different commercial GaAs digital

integrated circuits have been brought to the marketplace. These SSI and MSI logic circuits include NOR gates, Fan Out Buffers, Dual Comparitor, Precision D-Flip Flop (PDFF), several Frequency Dividers, and 8:1/1:8 MUX/DMUX chip set. Circuit yield and performance improvements have been observed over time as a result of the continuing learning curve in both design and manufacturing.

High speed performance of GaAs ICs is attributed to both material and device structure. A key figure of merit for performance is the transconductance (g_m) of the FETs. Figure 5 is a trend chart showing average g_m's for over 500 wafers from ~ 60 different wafer lots. Only one wafer was below 90 mS/mm (min. specification) with the average Gm distribution running from 120 mS/mm to ~ 125 mS/mm over the manufacturing period sampled. The present technology is capable of a solid 120 mS/mm transconductance. The present attainable FET transconductance in conjunction with a 1/4 τ_d divider circuit architecture provides for > 3 GHz operation. The histogram shown in Figure 6 shows an operating frequency distribution for ÷ 128 frequency dividers all operating above 2 GHz. As would be expected, there is a long monotonic rise in frequency of operation starting at 2 GHz, with the peak centered at 2.95 GHz, and a maximum operating frequency of 3.25 GHz.

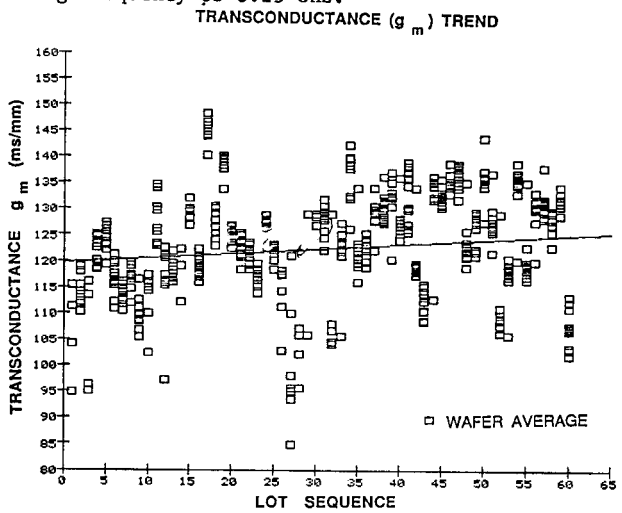

Fig. 5. Transconductance trend for 50 µm wide MESFETs.

Excellent progress has also been made in wafer sort yields. Figure 7 shows die yield for various size die areas. Currently GigaBit's products fall into three general die area sizes. The smallest SSI logic parts are ~ 2.8K mil^2, with MSI variable modulus dividers, ÷ 128, and PDFF parts at 5.7K mil^2 and MUX/DMUX chips at 11.5K mil^2. As can be seen from Figure 7, average wafer sort yields up to 73% (88% on the best wafer) are being experienced with over 50% observed on sophisticated (> 200 gates) MUX/DMUX logic parts. Current yield results on these size parts are slightly below what one would expect from similar size Si IC chips. However, Si IC yield predictions would be based on 2-3 µm geometries and very mature process and fabrication technologies.

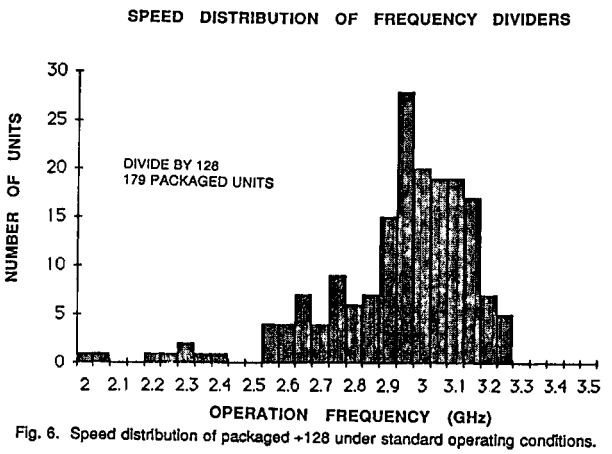

Fig. 6. Speed distribution of packaged ÷128 under standard operating conditions.

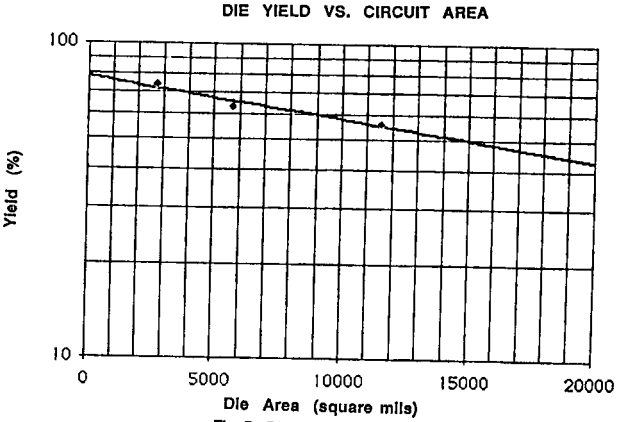

Fig. 7. Die yield vs. circuit area.

Yield And Reliability

The commercial manufacturing of GaAs MSI/LSI circuits demands high yield and reliable fabrication technology. Significant efforts have gone into designing a high yield process and verifying LSI yield compatibility as well as establishing GaAs reliability standards. A reliable, high yielding two level metal interconnect system is paramount in establishing a LSI process. Two aspects of such a system are the via contacts which connect first and second level lines and the interlevel dielectric and multi-level crossover isolation structures. Yield analysis test structures containing 18,900 crossovers each (36 structures / wafer) on engineering mask sets have resulted in outstanding results. Measurements have typically shown zero crossover failures (first to second level shorts) on greater than six million 2 µm wide first metal by 2 µm wide second level metal crossovers separated by 5000 Å of PE-CVD SiO_2. These measurements were conducted on 15 wafers randomly selected from two engineering lots. This excellent crossover yield is a direct result of the planar crossover process (see process discussion) used and the high integrity of the interlevel SiO_2.

In a sophisticated two level metal interconnect scheme, the more difficult job is insuring the connection between first and second interconnect lines by way of the via or contact window. Again, the use of a very planar via system, where

the via is filled with metal prior to the second metal deposition eliminates any potential for via side wall coverage problems. Figure 8 shows the via chain yield versus chain length for 2 μm x 2 μm via windows measured on 15 wafers. The yield of the via process can be modeled as:

$$Y_V = Y_0 (1 - D_V)^{N_V}$$

where Y_0 is the percentage of the wafer which is good, D_v is the probability of a via being defective, and N_V is the number of vias involved. Measurements of via chains for varying lengths have resulted in typical values of Y_0 = 99.54% and D_V = 6.54 x 10^{-6}. Further, the best wafer measured had 100% yield of via chains or 432,000 vias without a failure. This model predicts a yield of 87.35% for parts with 20,000 vias. For reference the 1K SRAM in development at GigaBit has ~ 15,000 vias. This type of specific yield analysis for GaAs IC structures strongly suggests that the manufacturing technology is maturing rapidly.

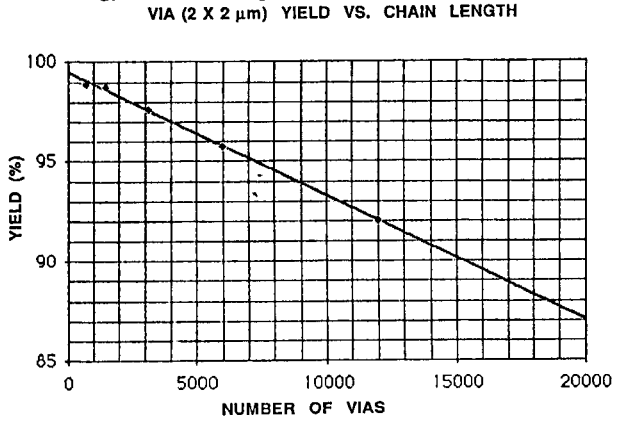

Fig.8. Via yield vs. number of vias (2μm x 2μm) in a chain.

The reliability and integrity of GaAs integrated circuits must be established before commercial market acceptance can take place. In response, a number of reliability studies and QA practices have been instituted at GigaBit Logic. Extensive storage tests at 250°C in nitrogen ambient have been conducted on standard IC wafer lots. In these tests, parametric measurements were initially taken and subsequently measured at various time points up to 2000 hours. Small changes in device parameters were occasionally noticed within the first hour at 250°C. In order to guarantee no drift in device parameters in subsequent testing and assembly, a stabilization bake was adopted in the process prior to wafer sort. At times up to 2000 hours, very little change in the basic device parameters; V_P, I_{DSS}, g_m, R_S, and R_C was observed. Ring oscillator yield was also found to be stable. This confirms that the present manufacturing process is free from thermally activated degradation up to temperatures of at least 250°C. Back-end processes such as die-mount, wire-bond and lid-seal employ temperatures < 250°C for short durations, thus ensuring parametric stability. Several hundred packaged ICs from various lots and product types have been subjected to static burn-in at junction temperatures (T_j) of 150°C. Based on a 6500 hour life-test on NOR gates, an MTBF of ≈ 40 million hours is predicted at normal operating temperatures, ie., T_j = 70°C. An even higher level of reliability is expected as the technology matures. To date, GaAs reliability studies have not observed any major failures and no major failure mechanism have yet been identified. The prognosis for GaAs IC reliability equal to or exceeding that of Si ICs is excellent.

Summary

GaAs IC manufacturing is finally coming of age providing for the long awaited promise of ultra high performance GaAs integrated circuits to become a commercial reality. A state-of-the-art three inch cassette to cassette FAB line has been established with adequate volume to achieve a reproducible and stable process technology. Designs and manufacturing methods have matured as evidenced by wafer sort yields approaching those experienced in Si ICs. Standardized wafer sort production testing, assembly, post-burn-in testing, and high speed testing operations have assured the customer stable parametric behavior and reliable high performance operation of GaAs IC prpoducts. Accelerated life tests and activation energy reliability studies continue to demonstrate the basic soundness and reliability of GaAs technology. Today GaAs ICs truly represent a high speed alternative to Si ICs.

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